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A Low Power Low Voltage High Performance CMOS Current Mirror

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Abstract
The current mirrors are one of the most important circuits in designing the analog and mixed-mode circuit. A low power and low voltage high-performance CMOS current mirror with optimized input and output resistance are presented in this paper. SPICE simulations confirm the high-performance CMOS current mirror with power supply close to the threshold voltage of the transistor. In this paper, for achieving the low input resistance and a very high output resistance, the combination of shunt input feedback and regulated cascode output stage are used.

Keywords: current mirror, SPICE, CMOS analog integrated circuits.

I. INTRODUCTION

Current mirrors with low power requirements are the core structure for almost all analog and mixed - mode VLSI circuit with a single supply which is nearly equal to the threshold voltage of the transistor. Now a day the low power circuit design is most desirable on the application of portable electronics. Reducing the power supply requirement is a straightforward technique to achieve low power consumption. At the large supply voltage, there is a tradeoff between speed, power, and gain. High-performance CMOS current mirror requires a very high output resistance and a low input resistance.

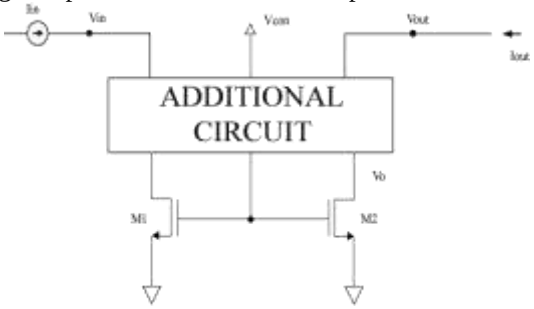


Fig.1. General block representation of high performance CMOS current mirror.

Here, in this paper, only n-MOS transistor current mirrors will be considered. All the considerations are applied to p-MOS current mirrors as well by changing the polarity of the voltages and currents. The general block representation of the high-performance CMOS current mirror is illustrated in Fig.1, all the area of discussion in this paper later on is dependent on this general block representation of high-performance COMS current mirror [1].

Description of Fig.1 is as two matched transistors, M1 as the input transistor and M2 as the output transistor and an additional circuitry. In the Fig.1, Vin is input voltage of current mirror, Vout is output voltage of current mirror, Vo is the voltage at drain of M2 and Vcon is the supply voltage for the control circuitry.

Some definitions and notations are applied throughout the paper. Those are index MIN/MAX stands for the minimum/maximum value which allows the appropriate operation of the current mirror, index [Q] stand for the quiescent condition, VTO is unbiased transistor's threshold voltage, VT is the threshold voltage of the transistor with body effect and VT > VTo. If the transistor M1 and transistor M2 is perfectly matched then VT of M1 = VT of M2 = VT. VDS(sat) is drain-source saturation voltage, VDS(sat) = VGS – VT, Vover is drain-source overdrive voltage, Vover = VDS – VDS(sat), and Av = gmro is the maximum gain of an amplifier, where gm is small signal transconductance gain and ro is the resistance of the transistor.

For demonstrative purpose, the typical values for 2 µm CMOS technology are set as, VTO = 0.75 V, Av = 75. Bias current and physical dimensions of transistor M1 & M2 are set to get VDS(sat)[Q] = 0.1 V and Vover[Q] = 0.05 V due to this the transistors M1 & M2 are in saturation mode and allow maximum gate to source voltage swing Vover[MAX] = 2Vover[Q] = 0.1 V with the drain to source voltage is constant.

Vmirror is the voltage required in the signal path which is nothing but the figure of merit with low voltage operations, in the case where some of the application required cascading of mirrors, which is given as Vmirror = Vin + Vout. Increasing the value

of the Vmirror significantly increased the performance of the mirror. For the conventional cascode mirror Vin[MIN] = 2VGS and Vout[MIN] = 2VGS – VT.

II. SOME HIGH PERFORMANCE CURRENT MIRROR SCHEMES

All the strategy for optimizing the input resistance and output resistance of a current mirror are based on the effectuation of shunt input and series output negative feedback amplifier. For this purpose, the input open loop gain is Aolinput and the output open loop gain is Aoloutput, then the input resistance will be Rin = 1/(gmlAolinput) and the output resistance will be Rout = ro2 Aoloutput.

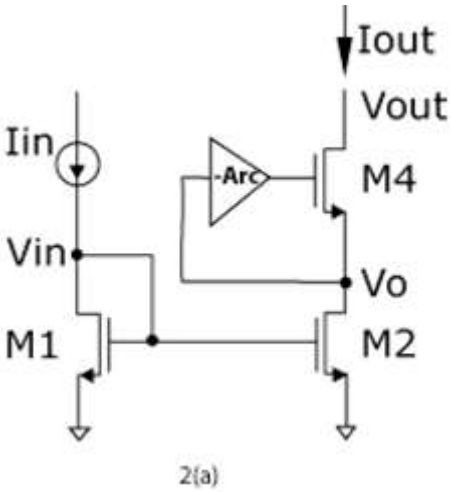
In Fig.2(a), the regulated cascode current mirror uses the –Arc gain amplifier to drive the next transistor. Due to this, a very high value of Aoloutput (= Av4Arc) is obtained, where Av4 is the voltage gain of the transistor M4, and, therefore a high output resistance is obtained [2].

Next circuit, Fig.2(b), is very similar to the previous circuit with the input voltage reduced by applying the feedback [3].

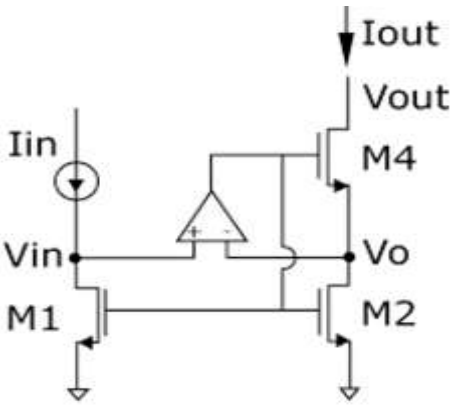
In the previous circuit and the next circuit, Fig.2(c), the accuracy of the current copy will improve by forcing VDS1 = VDS2 [4].

In the next scheme, illustrated in the Fig.2(d), the differential amplifier is implemented on both the input and output side of the current mirror. Reference voltage Vreference is connected to one of the inputs of both the amplifiers connected to the input and output side of the current mirror. This circuit has a good amount of high output resistance but lacks in low input resistance [5].

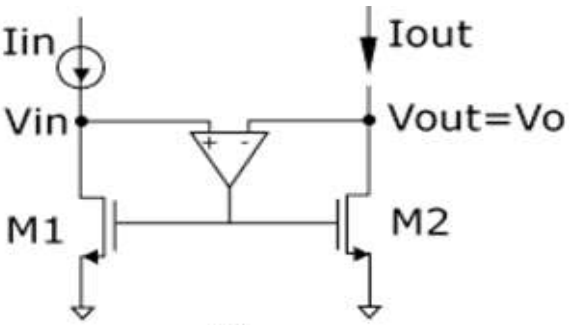
The scheme depicted in Fig.2(e) achieves low input resistance with low voltage requirements. This will achieve by implementing a shunt input scheme with a single ended amplifier with one transistor (M3) and one current source (Ib) with dc biased. Biased current is mirrored on the output of the current mirror [6].



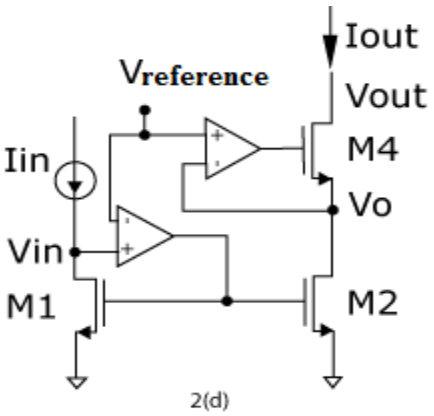
2(a)



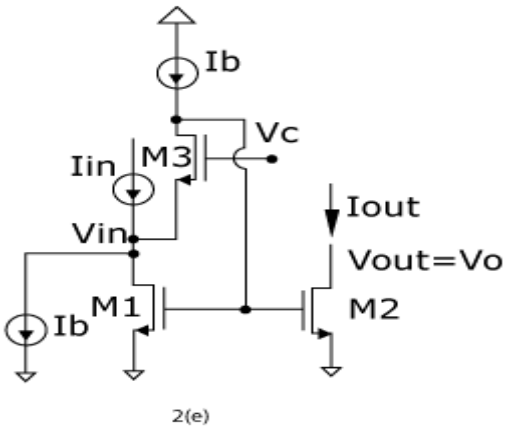
2(b)



2(c)



2(d)



2(e)

Fig.2. High performance current mirror schemes (a), (b), (c), (d) & (e)

III. HIGH PERFORMANCE CMOS CURRENT MIRROR SCHEME WITH LOW VOLTAGE REQUIREMENT

In this, a simple and efficient simulation of regulated cascode output section is hashed out. Extend to this a very high output resistance and precise current copy is achieved. The implementation is shown in the right half in the Fig.3(a). The differential amplifier Ada in a feedback loop is used in order to get the value of VDS1 equal to VDS2. This will improve the accuracy (it is given that the VGS & VDS of M1 & M2 is equal).

Differential amplifier with low voltage requirement is shown in fig.4, which includes a dc level shifter transistor M7 next to a differential pair transistor M5 and M6. Where the threshold voltage of n transistor is greater than the threshold voltage of p transistor, level shifter is required. The supply voltage of the amplifier is

Vconout[MIN] = Vo[MIN] + VSGM6[MIN] +VIbias[MIN]
= (VDS(sat)[Q] Vover[MAX]) + (|VTp| VDS(sat)[Q]) + …… ……VDS(sat)[Q]
= |VTp| + 3VDS(sat)[Q] + Vover[MAX]

(Assuming Vo = Vo[MIN] = VDS(sat)[Q] + Vover[MAX])

Where VTp is the threshold voltage of M5 and assuming the voltage drop VIbias[MIN] = VDS(sat)[Q] for the current source Ibias. When Vconout[MIN] is greater than Vconin[MIN], shows the minimum supply voltage requirements of a control circuit, Vcon.

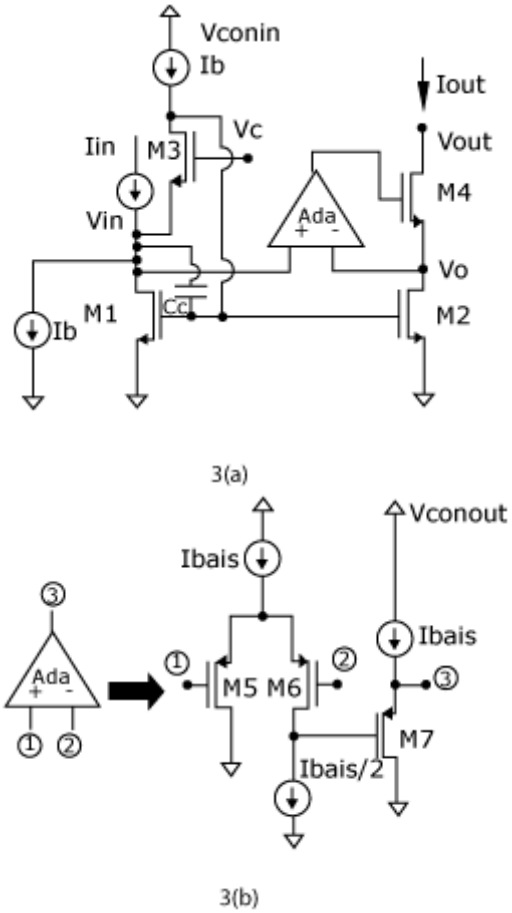


Fig.3. (a) Proposed high performance CMOS current mirror scheme with low voltage requirement, (b) Differential amplifier Ada.

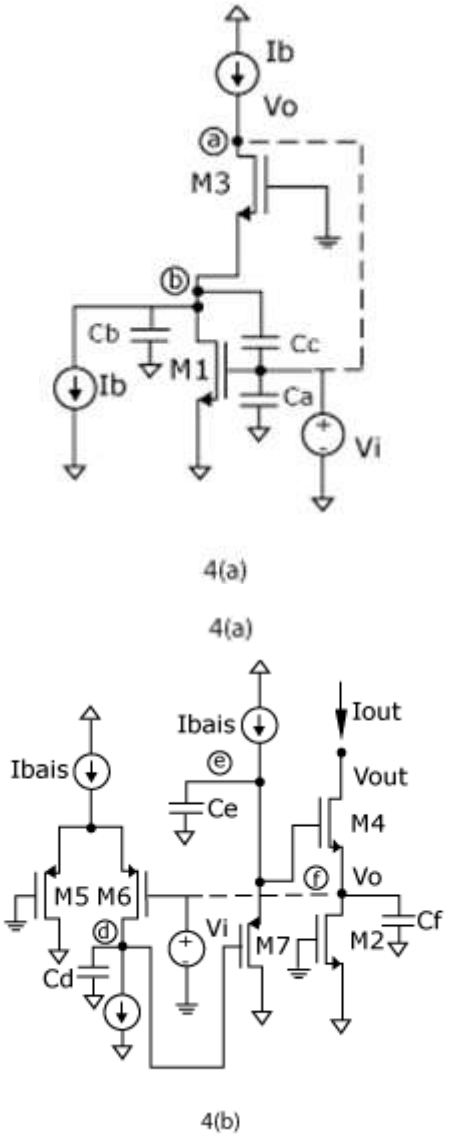


Fig.4. (a) Open loop response analysis at input, (b) Open loop response analysis at output

Coming back to the Fig.3(a), when M2 and M4 are in saturation and Vout > 2VDS(sat)[Q] + Vover[MAX], the output resistance is Rout = r02AdaAvM4, where Ada is the gain of differential amplifier and AvM4 (= gm4ro4) is the gain of M4 (cascode transistor). Let both the gains are equal in magnitude (50-100), then the output resistance takes the values in the giga-ohm range (in practical the values are in hundred Mega ohms due to the leakage of drain substrate current at the drain of transistor M4). For (VDS(sat)[Q] + Vover[MAX]) < Vout < (2VDS(sat)[Q] + Vover[MAX]), M4 leaves saturation region and open loop gain of output series feedback is decreased to Aolout = Ada. At this, still a high output resistance (Rout = ro2Ada) is achieved. Even for Vin, Vout < (VDS(sat)[Q] + Vover[MAX]) (M1 and M2 are in triode region) the current mirror is still in working with Rout = ro2. The last case is not in practical because the drain currents are dependent on VGS as well as VDS and due to this the offset voltages of the differential amplifier can contribute to comparatively large gain error.

Some disadvantages of this current mirror are, compared to the conventional high swing cascode current mirrors the low voltage requirement and optimized input and output resistance of this current mirror have come with additional circuit complexity, bandwidth limitations, power dissipation, transient performance and equivalent input noise degradation.

IV. SIMULATION RESULTS

The SPICE simulation of the frequency response shown in the Fig.5(a) with the parameters in Table 1. Here 2 µm CMOS process with threshold voltage 0.75 for nMOS and 0.8 V for pMOS is used. Equal bias current and base current were used for the current path of transistor M1, M2, M4 and for the transistor used in input and output control circuits. Fig. 5(a) shows the simulated frequency response and Fig. 5(b) shows the simulated time dependent response (transient response). The bandwidth of the current mirror is approximately 37MHz (close to 40 MHz). The parameters in Table 1 were selected such that we get overdrive voltage and drain to source saturation quiescent voltages of 0.1 V or less and 1.2 V supply for the control circuitry. The output dc characteristics of a current mirror were reported by sweeping output voltage (Vout) from 0 V to 1.2 V and input current from 4.2 µA to 8 µA as shown in Fig. 6(a). The measured input voltage (Vin) and output voltage (Vo) are approximately equal to 145 mV. The high output resistance (greater than 200 MΩ) was noted for Vout[MIN] greater than or equal to 0.22 V and current up to 10 µA, shown in Fig 6(b).

TABLE 1. Mirror parameters

W/L (µm) for all nMOS	25/2
W/L (µm) for all pMOS	50/2
Ibias (µA)	0.5
Ib (µA)	0.5
Vc (V)	0.95
Vcon (V)	1.2
RL (KΩ)	1
Cc (pF)	1

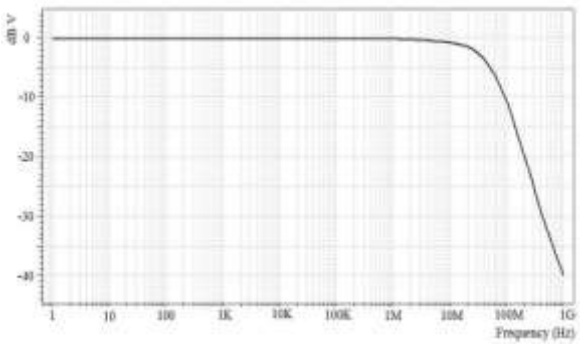


Fig.5(a)

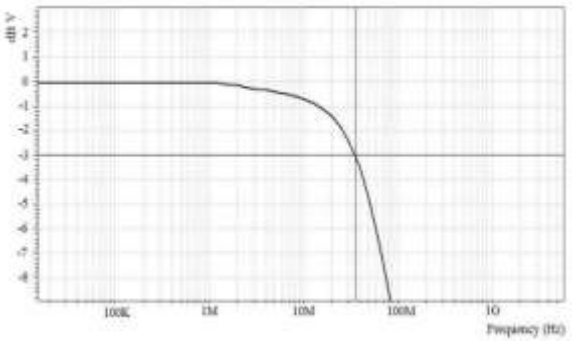


Fig.5(b)

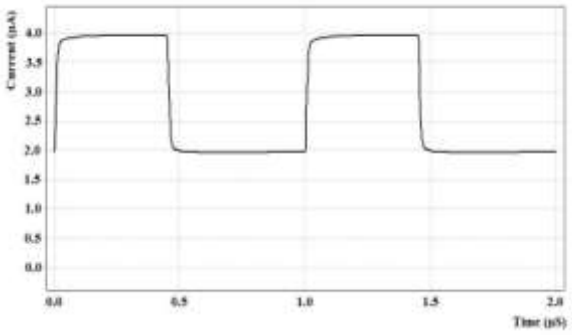


Fig.5(c)

Fig.5. Simulated responses (a) Frequency response, (b) Time dependent response.

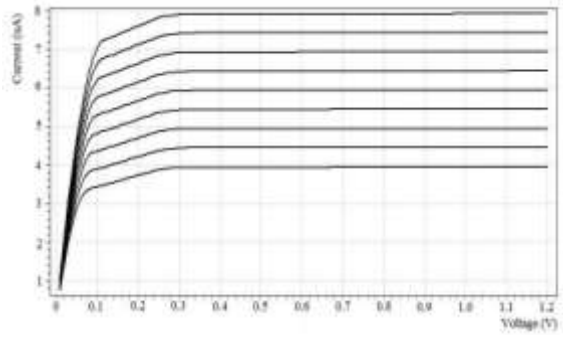
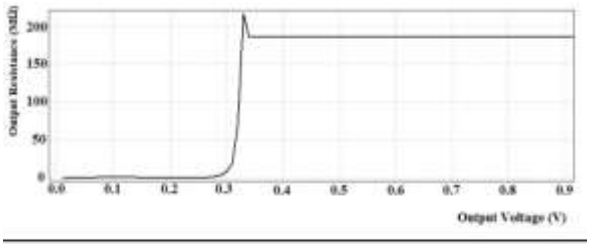


Fig.6(a)



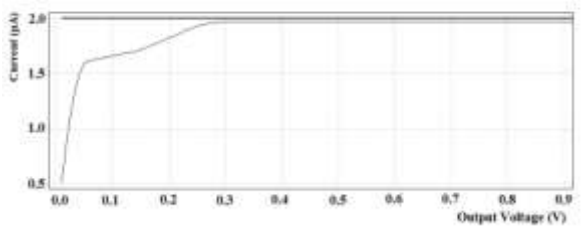


Fig. 6(b)

Fig.6. (a) Mirror's dc characteristics (b) Output impedance.

V. CONCLUSION

An efficient SPICE simulation of low voltage requirement high-performance current mirror was introduced. In this scheme, cascading mirrors with voltage requirement of just two times the minimum drain to source voltage of a transistor in saturation and optimized input and output resistances are obtained. The supply voltage requirements of the control circuitry are also close to the threshold voltage of a transistor. This current mirror circuit can be used as a basic structure for analog and mixed – mode VLSI circuits.

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